AMENDMENTS TO THE CLAIMS

The listing of claims below replace all prior versions, and listings, of claims:

1. (Currently Amended) A system comprising:

a memory bus; and

a plurality of memory controllers, each memory controller to generate memory requests on the memory bus according to a predetermined priority scheme, the predetermined priority scheme defining time slots, wherein the memory controllers are allocated to respective time slots according to the predetermined priority scheme,

at least two of the plurality of memory controllers adapted to generate concurrently pending memory requests on the memory bus in plural respective time slots.

2. (Cancelled)

3. (Cancelled)

4. (Original) The system of claim 1, wherein the memory bus comprises a Rambus channel.

5. (Original) The system of claim 1, wherein each memory controller generates a memory request during a different predetermined time slot.

6. (Original) The system of claim 1, wherein the memory bus comprises plural control portions, each of the control portions associated with corresponding time slot priority schemes.

7. (Original) The system of claim 6, wherein the time slot priority schemes are staggered.

8. (Original) The system of claim 6, wherein the control portion comprise a row portion and a column portion.

9. (Original) The system of claim 1, wherein the memory bus comprises plural portions, each portion associated with a set of memory devices.

10. (Currently Amended) A system comprising:

a plurality of memory buses ~~bus~~; ~~and~~

a hub connected to the plurality of memory buses; and

a plurality of memory controllers connected to a first one of the memory ~~bus~~ buses, each memory controller to monitor memory requests generated by another memory controller in performing memory-related actions,

the memory controllers to access a second one of the memory buses through the hub.

11. (Original) The system of claim 10, wherein the memory-related actions comprise a read-modify-write transaction.

12. (Original) The system of claim 10, wherein the memory-related actions comprise a cache coherency action.

13. (Original) The system of claim 10, wherein the memory-related actions comprise a memory request.

14. (Currently Amended) The system of claim 10, ~~the~~ each memory controller to determine if the memory buses are ~~bus is~~ available based on outstanding requests from other memory controllers.

15. (Currently Amended) A method for use in a system having plural memory buses, a hub connected to the memory buses, and a plurality of memory controllers, the method comprising:

~~providing multiple memory controllers on a memory bus;~~

generating requests, by the memory controllers, on the memory ~~bus~~ buses; and

each memory controller monitoring memory-related actions on the memory buses connected by the hub by at least another memory controller.

16. (Original) The method of claim 15, wherein generating the requests comprises generating Rambus command packets.

17. (Original) The method of claim 15, wherein generating the requests comprises the memory controllers generating the requests one at a time according to a predetermined priority scheme.

18. (Original) The method of claim 17, wherein generating the requests comprises generating the requests according to a time slot priority scheme.

19. (Original) The method of claim 17, wherein generating the requests comprises generating the requests according to a request-select priority scheme.

20. (Previously Presented) The method of claim 15, further comprising each memory controller determining when to generate a memory request based on the monitoring.

21. (Previously Presented) The method of claim 15, further comprising each memory controller determining if a lock has been asserted due to presence of a read-modify-write transaction.

22. (Previously Presented) The method of claim 15, further comprising each memory controller performing a cache coherency action based on the monitoring.

23. (Currently Amended) An article comprising one or more storage media containing instructions that when executed cause a memory controller to:

monitor memory requests from another memory controller on a memory bus;

~~determining~~ determine if a memory request can be generated on the memory bus based on the monitoring; and

generate memory requests on the memory bus according to a time slot priority scheme that defines time slots allocated to respective memory controllers.

24. (Previously Presented) The system of claim 1, wherein the plurality of memory controllers are connected to the memory bus.

25. (Previously Presented) The system of claim 1, wherein one of the at least two memory controllers is adapted to generate its memory request on the memory bus before data is returned for the memory request of the other one of the at least two memory controllers.

26. (Currently Amended) The system of claim 10, wherein at least two of the memory controllers are adapted to generate concurrently pending memory requests on the first memory bus, each of the concurrently pending memory requests comprising control information and memory address information.

27. (Currently Amended) The system of claim 26, wherein one of the at least two memory controllers is adapted to generate its memory request including control information and memory address information on the memory bus before data is returned for the memory request of the other one of the at least two memory controllers.

28. (Currently Amended) The method of claim 15, wherein generating the requests on the memory bus comprises at least two of the memory controllers generating concurrently pending requests on the memory bus, each of the concurrently pending requests comprising control information and memory address information.

29. (Currently Amended) The method of claim 28, wherein generating concurrently pending requests comprises one of the at least two memory controllers generating its request including control information and memory address information on the memory bus before data is returned for the request of the other of the at least two memory controllers.

30. (Previously Presented) The article of claim 23, wherein the memory controllers are connected to the memory bus.

31. (New) The system of claim 1, wherein the predetermined priority scheme enables the memory controllers to gain access to the memory bus without having to assert arbitration requests.

32. (New) The system of claim 1, wherein the memory controllers are adapted to access the memory bus according to a round-robin priority scheme.

33. (New) The system of claim 1, wherein the memory bus comprises a first memory bus, the system further comprising:

a hub connected to the first memory bus; and

a second memory bus connected to the hub, at least two of the memory controllers adapted to generate concurrently pending memory requests on the second memory bus through the hub.

34. (New) The system of claim 33, wherein each of the memory requests comprises control information and memory address information, the at least two memory controllers adapted to generate concurrently pending memory requests on the second

memory bus by providing control information and memory address information of the concurrently pending memory requests on the second memory bus.

35. (New) The system of claim 33, wherein each of the memory requests comprises control information and memory address information, the at least two memory controllers adapted to generate concurrently pending memory requests on the first memory bus by providing control information and memory address information of the concurrently pending memory requests on the first memory bus.

36. (New) The system of claim 10, wherein the plurality of memory controllers are each adapted to generate memory requests on the first one of the memory buses, each memory controller to monitor memory requests on the first one of the memory buses generated by another memory controller on the first one of the memory buses.

37. (New) The system of claim 10, wherein the plurality of memory controllers are each adapted to generate memory requests on the second one of the memory buses, each memory controller to monitor memory requests on the second one of the memory buses generated by another memory controller on the second one of the memory buses.

38. (New) The system of claim 37, wherein the memory controllers are adapted to access any of the memory buses according to a time slot priority scheme that defines a plurality of time slots allocated to respective memory controllers.

39. (New) The system of claim 38, wherein the memory controllers are adapted to access any of the memory buses according to the time slot priority scheme without asserting arbitration requests.

40. (New) The system of claim 10, further comprising memory devices connected to respective memory buses, the memory devices accessible by the memory controllers.

41. (New) The system of claim 11, wherein a first one of the memory controllers is adapted to generate the read-modify-write transaction, the first one of the memory controllers to assert a lock indication for a memory location accessed by the read-modify-write transaction to prevent another one of the memory controllers from accessing the memory location.

42. (New) The method of claim 15, further comprising:

the plurality of memory controllers generating memory requests on a first one of the memory buses; and

each memory controller monitoring memory requests on the first one of the memory buses generated by another memory controller on the first one of the memory buses.

43. (New) The method of claim 15, further comprising:

the plurality of memory controllers generating memory requests on a second one of the memory buses through the hub; and

each memory controller monitoring memory requests on the second one of the memory buses generated by another memory controller on the second one of the memory buses.

44. (New) The article of claim 23, wherein generating memory requests on the memory bus according to the time slot priority scheme is performed without generating arbitration requests.